Journal of Interfaces, Thin films, and Low dimensional systems 6 (1) Summer and Autumn (2022) 573-581

Design and analysis of binary CNFET-based VCO with adjustable frequency offset

Scientific research paper

Masoud Honaryar[1], Seied Ali Hosseini[2*], Seyyed Hossein Pishgar Komleh[1]

[1]*Department of Electrical Engineering, College of Technical and Engineering, West Tehran Branch, Islamic Azad University, Tehran, Iran*

[2]*Department of Electrical Engineering, College of Electrical Engineering, Yadegar-e-Imam Khomeini (RAH) Shahre Rey Branch, Islamic Azad University, Tehran, Iran*

ARTICLE INFO

Article history:
Received 4 March 2023
Revised 15 June 2023
Accepted 15 June 2023
Available online 27 June 2023

Keywords
Schmitt Trigger
Carbon Nanotube
Voltage Controlled Oscillator
Chirality Vector
Offset Frequency

ABSTRACT

This paper, in the first step, introduces a low-power oscillator in the GHz range using the CNFET technology with a Schmitt trigger, in which the upper trigger point and lower trigger point can be adjusted only through a change in the diameter of the nanotubes of two CNFETs. In this oscillator, the frequency and duty cycle of the output signal can be adjusted via a change in the physical parameters of the transistors and capacitor capacity. The relation of frequency based on physical parameters is analysed and obtained. The power consumption of the proposed oscillator at 2 GHz frequency is only 2.7 µWatt. In the second step, the proposed VCO is presented using the current mirror source and the body effect with only 12 CNFETs. The circuit has an output frequency variation range of 50 KHz to 3.5 GHz with a power consumption rate of 0.15 to 12 µWatts in the without offset mode. The ratio of the maximum frequency to the center frequency (fc) in the without offset mode is 1.95, which indicates the quality of linear changes of the output frequency. Through the use of frequency shift in with offset mode, we can access a wide range of frequency ranges by changing the input voltage. The proposed circuits are evaluated with the Stanford CNFET model at 32 nm technology in terms of output frequency linear range, power consumption and frequency stability against temperature and process variations are approved.

1 Introduction

In CMOS technology, problems such as short channel effect (SCE), tunnelling of electric charges and leakage current arise in the substrate due to the reduced dimensions of the transistor [1]. CNFET technology is one of the possible alternatives to CMOS technology [2]. This technology has a variety of advantages, including the increased conductivity, low power consumption, reduction of chip dimensions, better linear behaviour at high frequency and lower switching speed limitation [3]. Oscillator and VCO are widely used in analog, digital, and mixed-mode circuits. They include phase locked loops (PLLs) [4], [5], digital modulators, analog-to-digital converters (ADC), frequency synthesizers, and digital processors. Because of transferring the frequency bands of wireless and wire line telecommunication equipment to several tens of GHz, such as 5G technology, the common CMOS-based methods can no longer meet the application. However, CNFET technology, along with the modern oscillator design methods, can meet this application [6].

*Corresponding author.
Email address: Sal_Hosseiny@Yahoo.com
DOI: 10.22051/jitl.2023.43070.1083

Oscillator and VCO in the super-high-frequency (SHF) range have serious limitations in technology and manufacturing process. The design of oscillators is based on the three main methods of delay stage ring oscillator [7], [8], harmonic high-Q oscillators, including LC and crystal oscillators and oscillators based on Schmitt trigger. The use of LC oscillators increases the chip occupancy level and power consumption rate because of the presence of inductors [9]. The proposed oscillator in CNFET technology is designed and analysed based on Schmitt trigger, where LTP and UTP are directly dependent on diameter of thr carbon nanotubes of only two CNFETs [10].

By adding complementary elements, we introduce an oscillator in the GHz range whose output frequency and duty cycle depend on the physical characteristics of CNFET transistors and capacitor capacity. In the second step, by adding a voltage-to-current converter using the current mirror source and body bases, we present a VCO circuit with two offset and without offset modes widely used in the construction of PLL and digital modulators [11]. The results of simulation using the Stanford CNFET Model at 32 nm technology [12] show that the oscillator is stable with low-consuming in the GHz range. The output frequency of the VCO circuit has a suitable linear range which is stable to temperature and process variation.

2 Terminology

In CNFET transistors, we can control the density of current transfer between drain and source through carbon nanotubes by applying an electrostatic potential to the gate. These tubes are produced by torsion of graphene sheets in certain dimensions and directions. Graphene is an excellent alternative to conducting electricity instead of semiconductors due to its excellent properties in electrical conductivity, thermal conductivity, mechanical strength, and carrier mobility. Carbon nanotubes are classified into two categories: single wall CNT (SWCNT) and multi-wall CNT (MWCNT). The nanotube, depending on the torsion angle of the graphene sheet, exhibits different properties, resulting in the definition of chirality vector, which is denoted by the integer pair (n, m). In single wall CNT, the relationship between chirality vector coefficients and the diameter of a nanotube (D_{CNT}) is determined by Eq. (1) [13].

$$D_{CNT} = \frac{\sqrt{3}a_0\sqrt{n^2+nm+m^2}}{\pi}, \quad (1)$$

a_0 (≈0.142 nm) is the interatomic distance between each carbon atom with its neighbor. The nanotube is metallic if n=m or n-m=3i (i is an integer). Otherwise, the nanotube is a semiconductor. CNT's diameter (D_{CNT}) is inversely proportional to the threshold voltage (Vth), as shown in Eq. (2) [14,15].

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \approx \frac{0.436}{D_{CNT}(\eta m)}, \quad (2)$$

a (≈0.249 nm) is the lattice constant, e is the unit electron charge, Eg is the energy bandgap, and V_π (≈3.033ev) is the carbon π-π band energy in the tight bonding model. If m=0 is selected, the threshold voltage is calculated by Eq. (3). Since there is in CNFET, unlike CMOS, electrons and holes have same mobilities in CNT ($\mu_n \approx \mu_p$), thus CNFET channel n and channel p have almost the same performance in the output load drive [16].

$$V_{th} \approx \frac{5.492}{n}. \quad (3)$$

3 Proposed binary oscillator and binary VCO

In the proposed binary oscillator circuit shown in Fig. 1, M3, M4, M5 and M6 are two cross-coupled inverters that create a latch to hold the state [17]. M1 and M2 change the state in the value stored in the latch depending on the input voltage. The sum of the threshold voltages of M1 and M2 is greater than VDD so that hysteresis occurs. By selecting the chiral vector for M1 and M2 according to Eqs. (4) and (5), we can determine the approximate UTP and LTP values of the internal Schmitt trigger of the oscillator [10].

$$UTP \approx V_{th(M2)} = \frac{5.492}{n_2} = \frac{0.436}{D_{CNT(M2)\eta m}}, \quad (4)$$

$$LTP \approx V_{DD} - V_{th(M1)} = V_{DD} - \frac{0.436}{D_{CNT(M1)\eta m}}. \quad (5)$$

If n_1=n_2 for M1 and M2, the hysteresis curve of Schmitt trigger is symmetrical relative to $\frac{V_{DD}}{2}$ according to Eq. (6) [10].

$$\frac{LTP + UTP}{2} \approx \frac{V_{DD}}{2}. \quad (6)$$

The CIN is charged from the M7 path and discharged from the M8 path according to the state of the OUT node. The INPUT node voltage fluctuates alternately within the UTP and LTP bands. In the capacitor charging mode, VOUT=0, M8=off and M7=on. Ron(M7) and Ron(M8) are the on-state resistances of M7 and M8, respectively, which depend on the diameter and number of nanotubes.

The charging speed depends on the time constant τ_1=Ron(M7).CIN. As soon as the voltage of the INPUT node reaches UTP, the Schmitt trigger changes the state so that VOUT=1, M8=on, M7=off and the CIN is discharged from the M8 path. The discharge speed depends on the time constant τ_2=Ron(M8).CIN. When the voltage of the INPUT node reaches LTP, the Schmitt trigger changes again and VOUT = 0, M8 = off, M7 = on and the CIN is charged from the M7 path. By selecting the number of nanotubes for M7 and M8, we produce the ideal duty cycle.

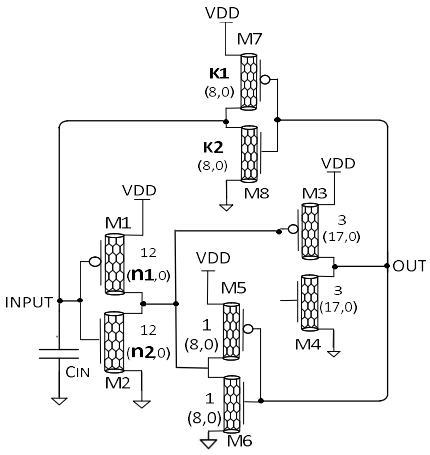

Figure 1.The proposed binary oscillator

Increasing the number of nanotubes for M7 and M8 (K1 and K2), result in the decrease of the Ron(M7) and Ron(M8) respectively. Figure 2 shows the output square wave and the charging and discharging waveforms of the input capacitor in an ideal mode. According to the charging and discharging curves of the capacitor in Figure 2, T1 and T2 are calculated according to Eqs. (7) and (8).

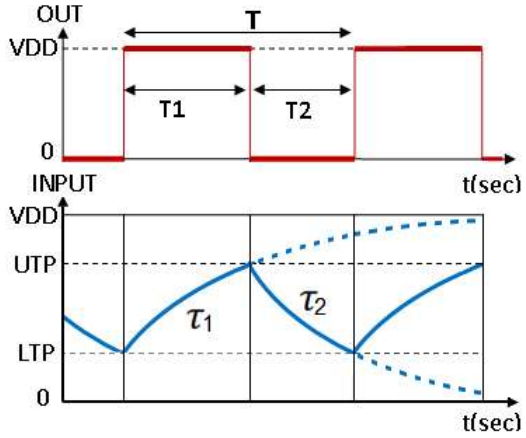

Figure 2. Ideal waveform for binary oscillator.

$$T_1 = \tau_1 . ln\left(\frac{LTP - V_{DD}}{UTP - V_{DD}}\right), \quad (7)$$

$$T_2 = \tau_2 . ln\left(\frac{UTP}{LTP}\right). \quad (8)$$

By substituting the nanotube diameter values from Eqs. (4) and (5) and time constants, T1 and T2 are calculated according to Eqs. (9) and (10).

$$T_1 = Ron(M7).C_{IN}.ln\left(\frac{\frac{0.436}{D_{CNT(M1)\,\eta m}}}{V_{DD} - \frac{0.436}{D_{CNT(M2)\eta m}}}\right), \quad (9)$$

$$T_2 = Ron(M8).C_{IN}.ln\left(\frac{\frac{0.436}{D_{CNT(M2)\,\eta m}}}{V_{DD} - \frac{0.436}{D_{CNT(M1)\eta m}}}\right). \quad (10)$$

If $D_{CNT} = D_{CNT(M1)} = D_{CNT(M2)}$ and Ron=Ron(M8)=Ron(M7) are selected, duty cycle=50% and the output frequency is calculated using Eq. (11). Otherwise, duty cycle≠50%. Thus, T1 and T2 times are calculated separately using Eqs. (9) and (10) and then the output frequency is calculated using Eq. (12).

$$f_{OUT} = \left[2Ron.C_{IN}\,ln\left(\frac{\frac{0.436}{D_{CNT(\eta m)}}}{V_{DD} - \frac{0.436}{D_{CNT(\eta m)}}}\right)\right]^{-1}, \quad (11)$$

$$f_{OUT} = \frac{1}{T_1 + T_2}. \quad (12)$$

Before introducing the proposed VCO circuit, three previously implemented VCO samples shown in Figure 3 are selected for comparison purposes. In the VCO circuit in Fig. 3(a), implemented in the primary circuit with 180 nm CMOS technology, a three-stage ring oscillator with the Barkhausen technique has been used to generate oscillations. For frequency control, current starved has been used as current control in the second stage [8]. In the VCO circuit in Fig. 3(b), which is implemented in the main circuit with the combined technology of CMOS (32 nm) and CNFET (32 nm), the Schmitt trigger along with the voltage-to-current converter has been used to control the charge and discharge currents of the capacitor [18]. In the VCO circuit in Fig. 3(c), implemented in the primary circuit with 45 nm CMOS technology, a five-stage ring oscillator has been used to generate oscillations. For frequency control, current starved has been used as current control in all five stages [19].

In all three circuits of Fig. 3, for a fair comparison, CNFET has been replaced by CMOS and simulated with 32 nm technology and then compared with the proposed binary VCO. In another comparison, three circuits in Figure 3 with the proposed binary VCO circuit are replaced and simulated by PTM 32 nm CMOS technology and the results are listed in Table 2 [20].

In the proposed VCO circuit shown in Fig. 4, the combination of the oscillator in Fig. 1 and voltage-to-current converter including M9, M10, M11 and M12 have been used. Connecting the OUT node to the body bases of M9 and M10 causes the dual function of these transistors in such a way that they act as part of the current mirror source to produce the charging and discharging currents of the CIN, and according to the OUT state, they determine the current path for charging or discharging the capacitor through the switching function. The circuit contains only 12 CNFETs and has with and without offset modes. Figure 5 shows the definition of an ideal VCO with and without offset. M11 and M9 are used as a current mirror source to produce the CIN charge current corresponding to the VCO-IN voltage. The CIN discharge current is supplied through the M10 corresponding to the VCO-IN input voltage. The diameter of the nanotubes in the voltage-to-current converter has been selected to be the same and equal to 1.33 nm for the symmetry of the charging and discharging state.

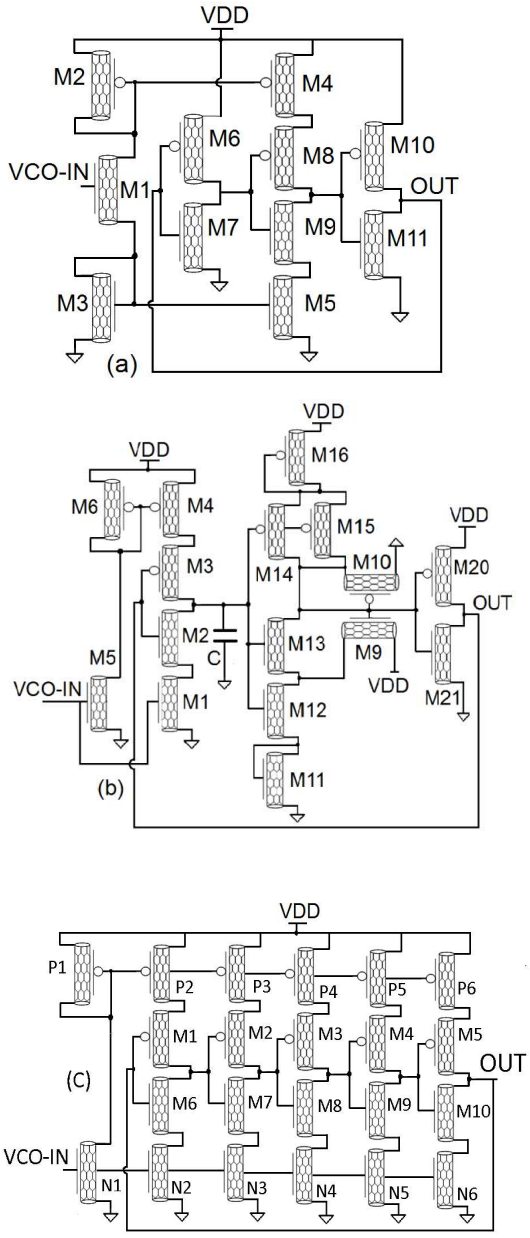

Figure 3. Related VCO with CNFET technology for comparison with proposed binary VCO (a) The VCO ref [8] (b) The VCO ref [18] (c) The VCO ref [19].

In order to achieve the minimum power consumption, we selected the number of nanotubes for M9, M10, M11, and M12 equal to 1. The SW switch is for selecting with and without offset modes. In the without offset mode, charging and discharging are done through the M9 and M10 paths, respectively. The output frequency depends on the capacity of the CIN, the

diameter of the M2, M1, M9, and M10 nanotubes, and the VCO-IN voltage.

In the SW=close state, the circuit is in with offset mode and charging is simultaneously done through M7 and M9 while discharging is done through M8 and M10. By selecting K as the number of M7 and M8 nanotubes, the level of vertical displacement of the curve in Fig. 5 is adjusted in the with offset mode.

In Fig. 5, fc is the VCO center frequency and K_{VCO} is the VCO ideal voltage-to-frequency converter coefficient defined by Eq. (13).

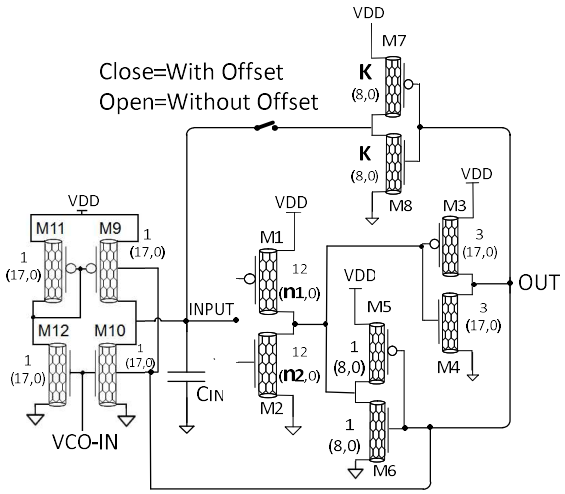

Figure 4. Proposed binary VCO circuit with CNFET technology.

$$K_{VCO} = \frac{f_{max} - f_{min}}{(VC0 - IN)_{max} - (VC0 - IN)_{min}} \qquad (13)$$

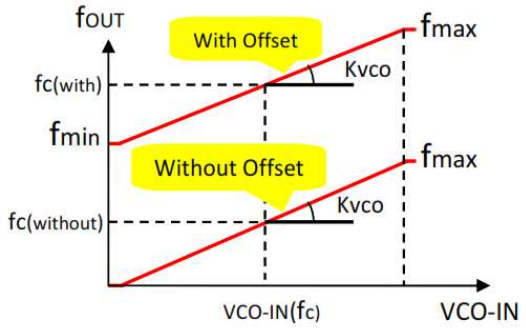

Figure 5. Definition ideal VCO with and without offset.

4 Simulation results

Simulations are performed based on Stanford CNFET model at 32 nm technology and Hspice software. In the oscillator shown in Fig. 1, by selecting n_1=n_2=10, which is obtained from Eqs. (4) and (5), UTP and LTP are obtained equal to 0.55 v and 0.35 v, respectively, and selecting CIN=4 fF and output load CL=0.5 fF in the OUT node, the simultaneous output and input waveform shown in Fig. 6. By selecting K1 and K2, you can see the desired duty cycle in the output.

Table 1 shows the values of output frequency, duty cycle, and power consumption according to the selected number of nanotubes for M7 and M8.

The approximately identical values of the power consumption show that the maximum power consumption occurs when the output signal level changes, and there is little power consumption at the output level stabilization mode.

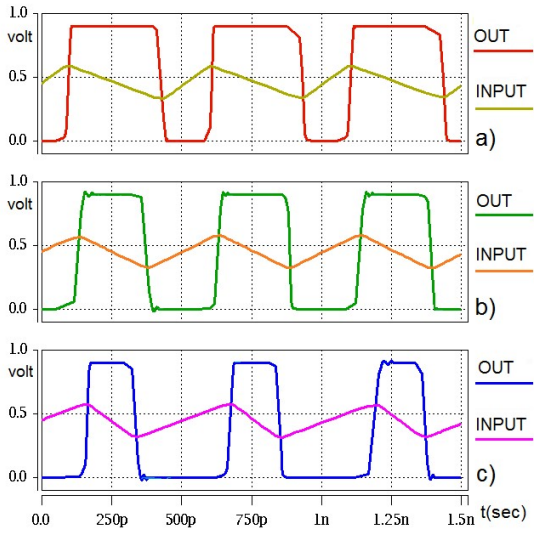

Figure 6. Out & input waveform of proposed binary oscillator (a) Duty Cycle>50% (b) Duty Cycle=50% and (c) Duty Cycle<50%

Table. 1. Simulation report of the proposed oscillator for Various choices K1 & K2.

VDD=0.9 v	*CL=0.5 fF*		*T=27°C*		*CIN=4 fF*
Proposed Oscillator	***K1***	***K2***	***Duty Cycle***	***fout (MHz)***	***Power Diss. (µW)***
Fig. 6.a	6	3	66%	1914	2.71
Fig. 6.b	4	4	50%	1882	2.75
Fig. 6.c	3	6	34%	1918	2.78

By selecting n_1=n_2=10 and CIN=1.5 fF with the output load CL=0.5 fF the VCO circuit of Fig. 4 (K=6) is simulated and compared with VCO circuits in Fig. 3 with the same technology, the comparison results are

presented in Table 2. Creating a desired offset by selecting the number of nanotubes for M7 and M8 is one of the unique features of the proposed VCO. Figure 7 shows the transfer characteristic for the proposed VCO in the three modes of without offset, with offset (K=3), and with offset (K=6) and the VCO circuits of Fig. 3 for comparison. The criterion for the K_{VCO} values in Table 2 is the statistical method of calculating the constant slope of the graphs of Fig. 7. Analyzing Table 2 and Fig. 7 enables us to make a fair comparison between the proposed circuit and the selected circuits.

Table. 2. Comparison of proposed binary VCO for different status with other works.

VDD=0.9 v	*CL=0.5 fF*	*T=27°C*	*CIN=1.5 fF*		
	VCO Without Offset	***VCO With Off. K=6***	***Fig. 3(a)***	***Fig. 3(b)***	***Fig. 3(c)***
fmin (MHz)	≈0	5050	370	≈0	23
fmax (MHz)	3521	6756	5400	2824	9050
fc (MHz)	1795	5847	1778	1372	4525
VCO-IN for fc	0.3 v	0.3 v	0.5 v	0.4 v	0.6 v
K_{VCO} (MHz/mv)	6.52	3.04	9.25	4.30	21.5
Power diss.for fc (µW) CNFET(32n)	1.9	5.8	1.1	3.6	6.6
Power diss.for fc (µW) CMOS(32 n)	10	33.3	2.3	6.7	44.5
Power diss. for fmax (µW) CNFET(32n)	12.3	15.9	6.3	13	15.5
Power diss. for fmax (µW) CMOS(32 n)	38.2	43.8	8.7	34.5	101

The significant change of the proposed VCO output frequency starts from VCO-IN=0.1 v, while it starts from VCO-IN=0.2 v for the circuit of Fig. 3(b) and in Fig. 3(a) for an input of less than 0.2 v, the signal generated with its distortion and amplitude is negligible. The significant change of the Fig. 3(c) output frequency starts from VCO-IN=0.3 v.

The frequency range of the proposed circuit output is very diverse with the possibility of selecting offset and capacitor. The power consumption shown in Table 2 at the maximum frequency and at the center frequency in the two modes of the proposed circuit is in proper condition compared to the selected circuits.

In Table 2, the proposed VCO circuit for different status has been simulated along with comparison circuits with PTM low power 32 nm CMOS technology, which shows the significant superiority of 32 nm CNFET technology in terms of power consumption.

Figure 8 shows the variation of frequency versus the input voltage in the range of 0 to 100mv. As can be seen the proposed circuit is more sensitive than the circuit of Fig. 3(b). Also, circuits of Figs. 3(a) and 3(c) cannot generate output in this range. In both circuits, the input transistor is located in the sub-threshold conduction region. In the proposed design, depending on the input range between 0 and 100 mv, the output frequency changes in a much larger range compared to the circuit in Fig. 3(b).

This unique property defines a wide range of instrumentation applications for the proposed circuit and can be used as a direct converter between a variety of sensors and processors.

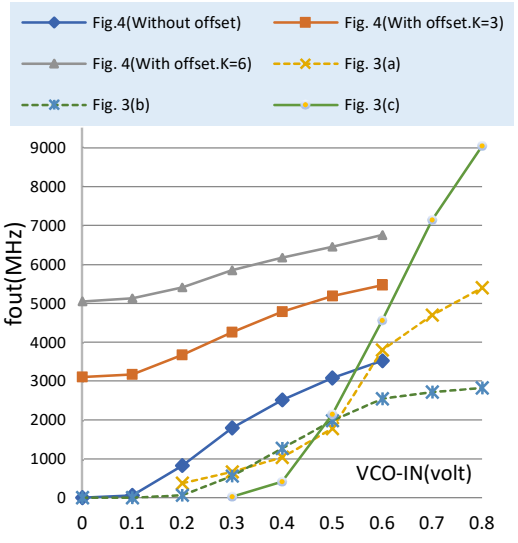

Figure 7. Comparison of frequency vs VCO control voltage curve for proposed binary VCO with different status and other works.

According to the graphs in Figs. 5 and 7, the center frequency (fc) of the proposed VCO occurs approximately at the VCO-IN=0.3 V input range. Figure 9 depicts the thermal stability of the center frequency with respect to temperature changes in the range of 0 to 100°C with steps of 10°C (for condition VCO-IN=0.3 v and CIN=1.5 fF). As can be seen, an increase in the temperature causes a slight increase in the center frequency of the VCO.

At the nanoscale, Proces variation can seriously affect product performance. In the Monte Carlo analysis, the stability of the center frequency (fc) for the proposed VCO has been measured in three modes and during the process variations with ±5 to ±15% Gaussian distributions. The stability results against process variation are presented in Fig. 10.

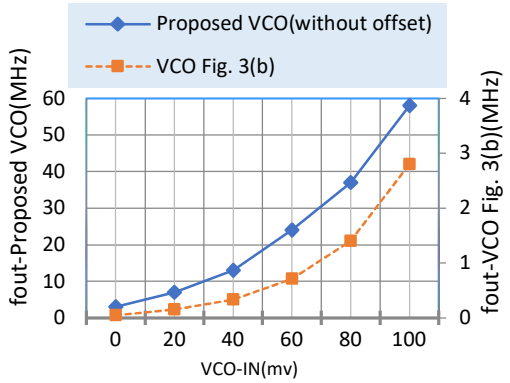

Figure 8. Effect of VCO-IN small variation on frequency in the proposed VCO without offset and VCO Fig. 3b.

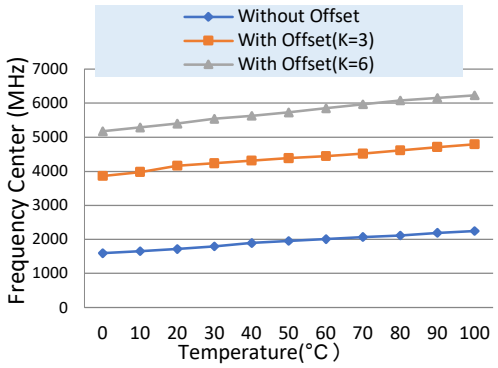

Figure 9. Center frequency deviation vs temperature variation for proposed VCO with different status with & without offset.

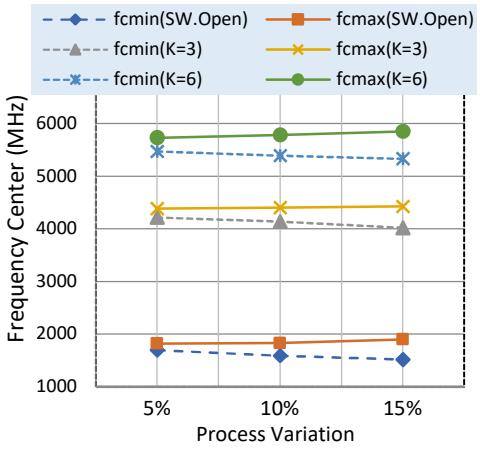

Figure 10. Frequency center deviation vs process variation for the proposed VCO with different status with and without offset.

5 Conclusions

In this paper, by selecting a suitable Schmitt trigger, we proposed an oscillator with a wide range of applications in clock pulse-based circuits according to the simple adjustment of frequency and duty cycle. The proposed low-power oscillator can be a suitable candidate which is needed for reliable frequency generators in the range of several tens of GHz in the future. Then, we proposed the VCO circuit with only 12 transistors. The circuit has a suitable linear range, also thanks to the possibility of creating a frequency offset, it can improve the performance of digital tuners and frequency synthesizer circuits both in a free-running way and in the PLL structure. The proposed VCO circuit has a high sensitivity to the input voltage around zero voltage. This property defines another application for the circuit to directly send measurements from a wide range of sensors to the processing unit. The simulation results show that the circuit has proper stability at high frequencies.

References

[1] C. Codreanu, E. Vasile, E. Iliescu, M. Avram, A. Badoiu, and C. Ravariu, “Free carrier lifetime reduction in silicon by electron-beam irradiation.” 23rd IEEE International Semiconductor Conference (CAS 2000). Location: Sinaia, Romania, **255** (2000) 10.

[2] S. I. Sayed, M. M. Abutaleb, and Z. B. Nossair, “Optimization of CNFET parameters for high

performance digital circuits." Advances in Materials Science and Engineering, **2016** (2016) 6303725.

[3] A. U. Alam, C. M. S. Rogers, N. Paydavosi, K. D. Holland, S. Ahmed, and M. Vaidyanathan, "RF linearity potential of carbon-nanotube transistors versus MOSFETs." IEEE transactions on nanotechnology, **12** (2013) 340.

[4] Y. Kumar, A. Raman, R. Ranjan, and R. K. Sarin, "High-frequency CNTFET-based voltage-controlled oscillator for PLL application." Micro-Electronics and Telecommunication Engineering. Micro-Electronics and Telecommunication Engineering pp 413–419 (Springer Link) (2020)

[5] E. Abiri and A. Darabi, "A novel modified GDI method-based clocked M/S-TFF for future generation." Microprocessors and Microsystems, **60** (2018) 122.

[6] C. Rutherglen and et al., "Wafer-scalable, aligned carbon nanotube transistors operating at frequencies of over 100 GHz." Nature Electronics, **2** (2019) 11.

[7] M. Khaleqi Qaleh Jooq, A. Bozorgmehr, and S. Mirzakuchaki, "A low-power delay stage ring VCO based on wrap-gate CNTFET technology for X-band satellite communication applications." International Journal of Circuit Theory and Applications, **49** (2021) 142.

[8] A. Ramazani and et al., "CMOS ring oscillator with combined delay stages." International Journal of Electronics and Communications (AEÜ), **68** (2014) 515.

[9] B. Jafar and S. Sheikhaei, "Low phase noise LC VCO with sinusoidal tail current shaping using cascade current source." International Journal of Electronics and Communications (AEÜ), **83** (2018) 114.

[10] M. Honaryar, S. A. Hosseini, and S. H. A. Komleh, "A novel model of binary and ternary Schmitt triggers based on multi-threshold voltage in nanoelectronics." International Journal of Electronics and Communications (AEÜ), **137** (2021) 153804.

[11] H. Sarbazi, R. Sabbaghi-Nadooshan, and A. Hassanzadeh, "A CNT based VCO with extremely low phase noise and wide frequency range for PLL application." International Journal of Numerical Modelling, **34** (2021) 5.

[12] Stanford university CNFET model website (2008). Stanford university, stanford, CA [Online]. Available: http://nano.stanford.edu/model.php?id=23

[13] M. Ghelichkhan, S. A. Hosseini, and S. H. P. Komleh, "Multi-digit binary-to-quaternary and quaternary-to-binary converters and their applications in nanoelectronics." Circuits, Systems and Signal Processing, **39** (2020) 1920.

[14] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field effect transistors Including non-Idealities and its application-Part I: Model of the intrinsic channel region." IEEE Transactions on Electronic Devices, **54** (2007) 3186.

[15] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field effect transistors Including non-idealities and its application-Part II: Full device model and circuit performance benchmarking," IEEE Trans. Electron Devices, vol. 54, no. 12, pp. 3195-3205, Dec. 2007

[16] M. H. Moaiyeri, K. Navi, and O. Hashemipour, "Design and evaluation of CNFET- based quaternary circuits." Circuits, Systems, and Signal Processing, **31** (2012) 1631.

[17] N. Weste and K. Eshraghian, "Principles of CMOS VLSI design." (A systems perspective), 2nd ed. reading, MA: Addison Wesley, 1993

[18] H. Ghanbari Khorram and A. Kokabi, "Proposed 3.5 mW CNTFET-MOSFET hybrid CSVCO for power-efficient gigahertz applications." Circuit World, **46** (2020) 193.

[19] A. Nakhale, M. N. Thakare, and N. M. Chore, "Physical design of VCO with wide frequency tuning range using deep submicron CMOS technology." International Journal for Research

in Applied Science & Engineering Technology (IJRASET), **10** (2022) 1177.

[20] J. Borgmans, R. Riem, and P. Rombouts, Senior Member, "The analog behavior of pseudo digital ring oscillators used in VCO ADCs." IEEE Transactions on Circuits and Systems." **68** (2021) 2827.